



mas A. Figura

Title:

METHOD AND STRUCTURE FOR IMPROVED ALIGNMENT TOLERANCE IN MULTIPLE,

SINGULARIZED PLUGS

Docket No.:

303.645US2

Filed:

December 4, 2001

Examiner:

Serial No.: 10/004,656

Due Date: March 4, 2002

Group Art Unit: 2813

Commissioner for Patents Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

 $\frac{\mathbf{X}}{\mathbf{X}}$ A return postcard.

A Preliminary Amendment (3 Pages).

n additional fee is required due to changes to the claims, the fee has been calculated as follows:

		CL	AIMS AS AMENDE	D		,
	(1) Claims Remaining After Amendment		(2) Highest Number Previously Paid For	(3) Present Extra	Rate	Fee
TOTAL CLAIMS	34	-	22	12	x 18 =	\$216.00
INDEPENDENT CLAIMS	6	-	3	3	x 84 =	\$252.00
[] MULTIPLE DEPENDENT CLAIMS PRESENTED						\$0.00
TOTAL						\$468.00

Please charge the required fee of \$468.00 to Deposit Account No. 19-0743.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 22 day of February, 2002.

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(GENERAL)





Unknown

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Thomas A. Figura

Examiner: Unknown

Serial No.:

10/004,656

Group Art Unit: Unknown

PATENT

Filed:

December 4, 2001

Docket: 303.645US2

Title:

METHOD AND STRUCTURE FOR IMPROVED ALIGNMENT TOLERANCE

IN MULTIPLE, SINGULARIZED PLUGS

PRELIMINARY AMENDMENT

Commissioner for Patents Washington, D.C. 20231

When the above-identified patent application is taken up for consideration, please amend the application as follows:

IN THE CLAIMS

Please add the following new claims:

23. (New) An integrated circuit device comprising:

first and a second surface structures, each having a top surface;

an inner plug located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a pair of outer plugs, each having an upper portion covered the top surface of one of the first and second surface structures;

an inner electrical contact connected to the inner plug; and

a pair of spacers for separating the inner plug and the inner electrical contact from the pair of outer plugs.

- 24. (New) The integrated circuit device of claim 23 further comprising a substrate connected to the first and second surface structures, the inner plug, and the pair of outer plugs.
- 25. (New) The integrated circuit device of claim 24, wherein the first and second surface structures are spaced apart along the substrate.